In the Claims:

1. (Previously Presented) A method of transferring programming instructions from a first memory disposed on a substrate, to a plurality of integrated circuits (ICs) disposed on the substrate and communicatively coupled to one another through test circuitry that provides debugging capabilities, comprising:

a first one of the plurality of ICs

accessing the first memory,

retrieving a first set of programming instructions, and

storing the first set of programming instructions within the first one of the plurality of ICs; and

the first one of the plurality of ICs

accessing the first memory,

retrieving a second set of programming instructions, and

transmitting, using the test circuitry, the second set of programming instructions to a second one of the plurality of ICs.

2. (Previously Presented) The method of claim 1, wherein the first and second ones of the plurality of ICs each comprises a processor capable of executing, respectively, the first and second sets of programming instructions and further including the step of debugging the plurality of ICs using the test circuitry by operating the test circuitry in a test mode and wherein the each of the steps of accessing retrieving, storing and transmitting is implemented when the test circuitry is in a mode other than the test mode.

3. (Previously Presented) The method of claim 2, further comprising the first one of the plurality of ICs executing at least a portion of the first set of programming instructions; in a test mode, operating the test circuitry using control signals from a source external to the substrate, and in a mode other than the test mode, operating the test circuitry using control signals generated on the substrate.

4. (Original) The method of claim 3, wherein executing at least a portion of the first set of programming instructions occurs prior to transmitting the second set of programming instructions to a second one of the plurality of ICs.

5. (Original) The method of claim 2, further comprising the first one of the plurality of ICs accessing the first memory, retrieving a first set of data, and storing the first set of data within the first one of the plurality of ICs; and the first one of the plurality of ICs accessing the first memory, retrieving a second set of data, and transmitting the second set of data to a second one of the plurality of ICs.

6. (Previously Presented) The method of claim 3, wherein the substrate comprises a printed circuit board, and the test circuitry of each of the plurality of ICs has an input for a test mode signal and a clock that is common to each of the plurality of ICs.

7. (Original) The method of claim 3, wherein transmitting comprises serially shifting data out from the first integrated circuit and concurrently shifting data in to the second integrated circuit.

8. (Original) The method of claim 7, further comprising transmitting control information from the first integrated circuit to the second integrated circuit prior to transmitting the second set of programming instructions to a second one of the plurality of ICs.

9. (Original) The method of claim 8, wherein the control information directs the second one of the plurality of ICs to receive a subsequent transmission of programming instructions.

10. (Previously Presented) In a system including a plurality of integrated circuits (ICs) disposed on a printed circuit board, each IC having a memory for storing at least programming instructions, test circuitry for providing debugging functionality, and a processor coupled to the memory for executing programming instructions stored in the memory; the system further including a single non-volatile memory disposed on the

printed circuit board and coupled for memory access to only a first one of the plurality of ICs, a method of downloading code from the single non-volatile memory to each of the plurality of ICs, comprising:

receiving, at a first one of the plurality of ICs, a first set of data from the single non-volatile memory;

storing the first set of data in the memory of the first one of the plurality of ICs;

receiving, at the first one of the plurality of ICs, a second set of data from the single non-volatile memory;

transmitting, using the debugging circuitry, the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and

storing the second set of data in the memory of the second one of the plurality of ICs, wherein the first and second sets of data comprise program code.

11. (Previously Presented) The method of claim 10, further comprising: executing, in the first IC, at least a portion of the program code in the first set of data; receiving, at the first one of the plurality of ICs, a third set of data from the single non-volatile memory; transmitting the third set of data from the first one of the plurality of ICs to a third one of the plurality of ICs; and storing the third set of data in the memory of the third one of the plurality of ICs.

12. (Previously presented) The method of claim 10, wherein transmitting the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs comprises serially shifting data out of the first one of the plurality of ICs via an output terminal; wherein the output terminal is coupled to an input terminal of the second one of the plurality of ICs, the input terminal coupled to circuitry within the second one of the plurality of ICs that is adapted to receive serial data.

13. (Previously Presented) The method of claim 12, further comprising placing the test circuitry in a test mode and providing transmitting control information from the first one of the plurality of ICs to the second one of the plurality of ICs prior to transmitting the second set of data.

14. (Original) The method of claim 13, wherein control information is transmitted in accordance with a JTAG standard of communication.

15. (Previously Presented) An electronic product, comprising:

a first integrated circuit having

a first processor,

a first internal memory,

a first test circuit including a first serial communication interface, and

an external memory interface;

an external memory coupled to the external memory interface;

a second integrated circuit having

second processor,

a second internal memory, and

a second test circuit including a second serial communication interface,

the second serial communication interface being coupled to the first serial communication interface;

wherein the first integrated circuit, the external memory, and the second integrated circuit are disposed on a substrate and wherein the first test circuit and the second test circuit are configured and arranged to communicate debugging information in a test mode and to communicate code images in another mode.

16. (Original) The electronic product of claim 15, wherein the first processor is coupled to the first internal memory, the first internal memory is adapted to receive a first code image, the second processor is coupled to the second internal memory, the second internal memory is adapted to receive a second code image, and the external memory is a non-volatile memory encoded with the first and second code images.

17. (Original) The electronic product of claim 16, wherein the first integrated circuit includes a first hardware facility for performing at least a first function, and the second integrated circuit includes a second hardware facility for performing at least a second function, and the first and second functions are different.

18. (Original) The electronic product of claim 17, further comprising a third integrated circuit, having a third processor, a third internal memory, and a third serial communication interface, the third serial communication interface being coupled to the second serial communication interface, the third processor coupled to the third internal memory, the third internal memory is adapted to receive a third code image, and the external memory further encoded with the third code image.